Passive Localization Algorithm using a Highly Integrated Acoustic Sensor Array

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UW-STREAM
Underwater Sensing and Transmission using Electro-Acoustic Modems

Motivation

There is significant interest to increase our access to the Earth's oceans, to discover and exploit its resources in a sustainable fashion. To monitor the environment, instruments are moored at the bottom of the ocean and are mounted with heterogeneous sensors. The choice of sensor array size depends on the available space, the power consumption, and the data processing capability. <u>In this work, a remote acoustic sensor array is proposed to detect and localize marine mammals.</u>

Research Objectives

- Develop a <u>small form-factor</u>, <u>low-power</u> acoustic sensor for harbour porpoise localization.
- <u>Compute in real-time the localization</u> algorithm on a System-on-Chip (SoC).
- Implement the peripherals in VHDL and develop the controller in the PetaLinux operating system.
- Compare the real-time algorithm with a MATLAB simulation to demonstrate the potential for the remote platform to reliably detect marine mammals.
- Evaluate and optimize the resource and power requirements of the implemented SoC design.

Fig. 1:Five-element Acoustic Sensor Array Recorder

Fig. 2: Harbour Porpoise

Localization Algorithm Calculations

The localization algorithm is implemented using the following three equations:

1. Propagation model which is the superposition of the two arrivals of the signal s with different gains α and arrival times τ.

$$r_n(t) = \alpha_0(p_0, p_n) \cdot s\left(t - \tau_{0,n}(p_0)\right) + \alpha_1(p_0, p_n) \cdot s\left(t - \tau_{1,n}(p_0)\right)$$

2. The cross-correlation matrix between channel estimated transmit signal and a hypothetical source at test position p.

$$C_c(p) = \frac{1}{L}\sum_{k=0}^{L-1}\left(\bar{s}^{\top}(t_k, p)\bar{s}(t_k, p)\right)$$

3. Estimate source position $\widehat{p_0}$ by determining the test source position p which leads to the lowest determinant of the cross-correlation matrix C_c.

$$\widehat{p_0} = \arg\min_{p}\{det[C_c(p)]\}$$

System-on-Chip Architecture

- On the Zybo Z7-20 combining ARM Cortex-A9 Processor with a Xilinx Artix-7 FPGA.
- Three main layers to create a real-time localization system:
  - **Communications:** algorithm parameters through UART interface and channel measurements through ethernet interface.
  - **Zynq Processor:** software used to drive the FPGA and provide updates to the map display.
  - **VHDL Peripherals**: hardware peripherals used to perform localization, including the propagation model of the environment.

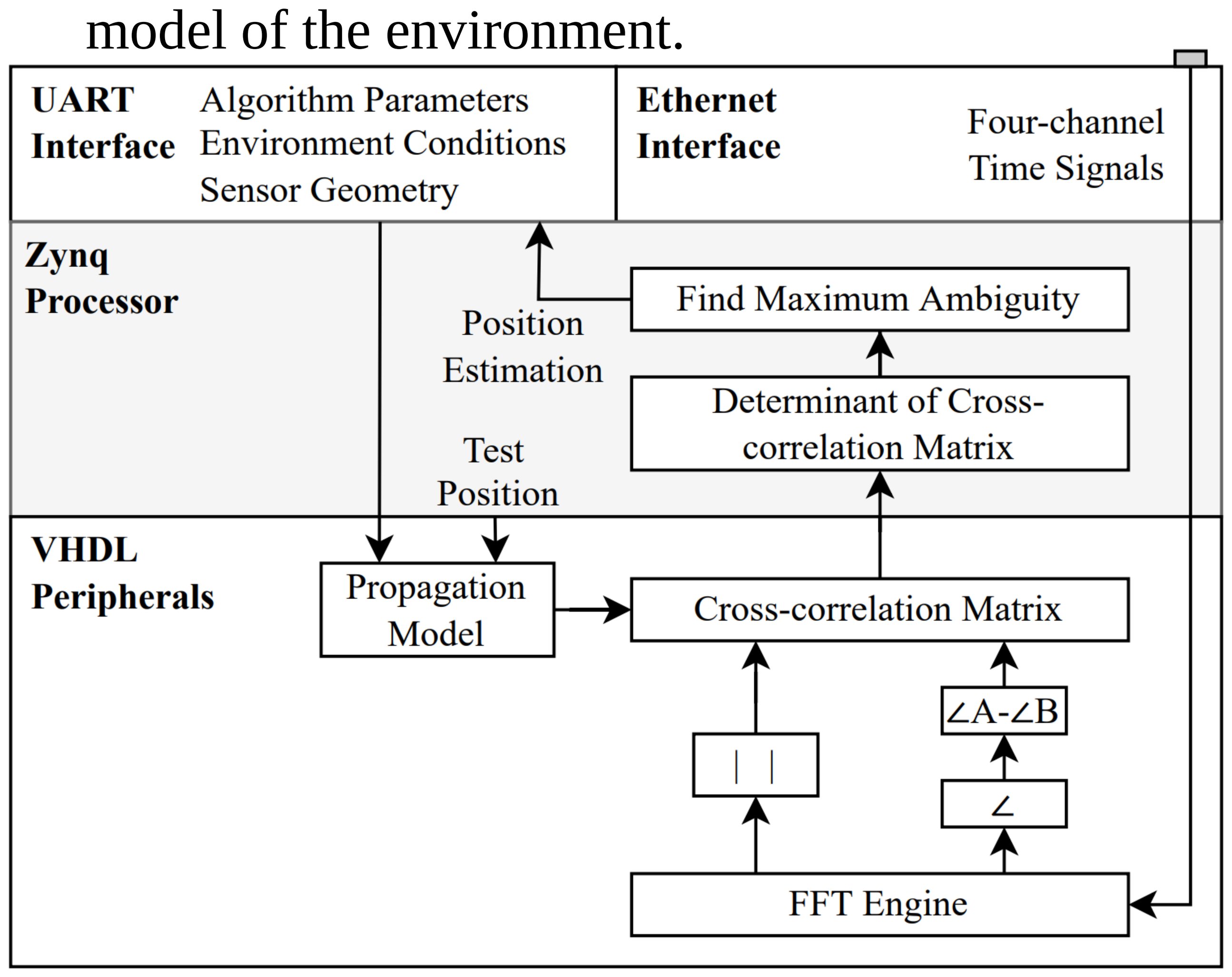

Fig. 3: System-on-Chip Architecture

System-on-Chip Implementation

- Uses fixed-point and floating-point representation depending on the expected scale of operations.
- Uses the Coordinate Rotation Digital Computer (CORDIC) and Fast Fourier Transform (FFT) IP-Cores provided by Xilinx to obtain the phase relationship (arctangent) between signals.

System-on-Chip Results

- Accuracy of the implemented SoC was evaluated by comparing the ambiguity function obtained using the FPGA and a MATLAB simulation.

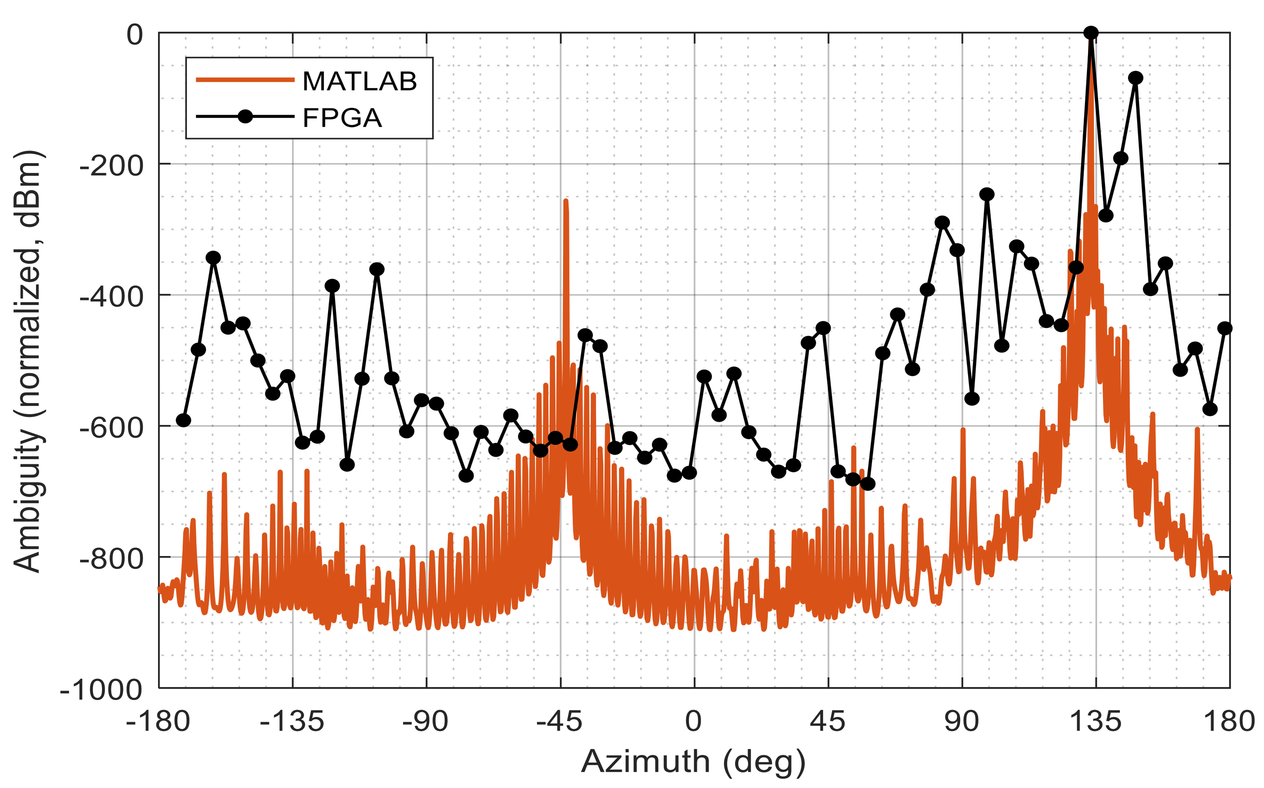

Fig. 4: Ambiguity Function of the Real-Time System

Fig. 5: Deployed Five-element Platform

Localization Algorithm Results

- Proposed algorithm compared to standard Time Difference of Arrival (TDoA) using a simulation.

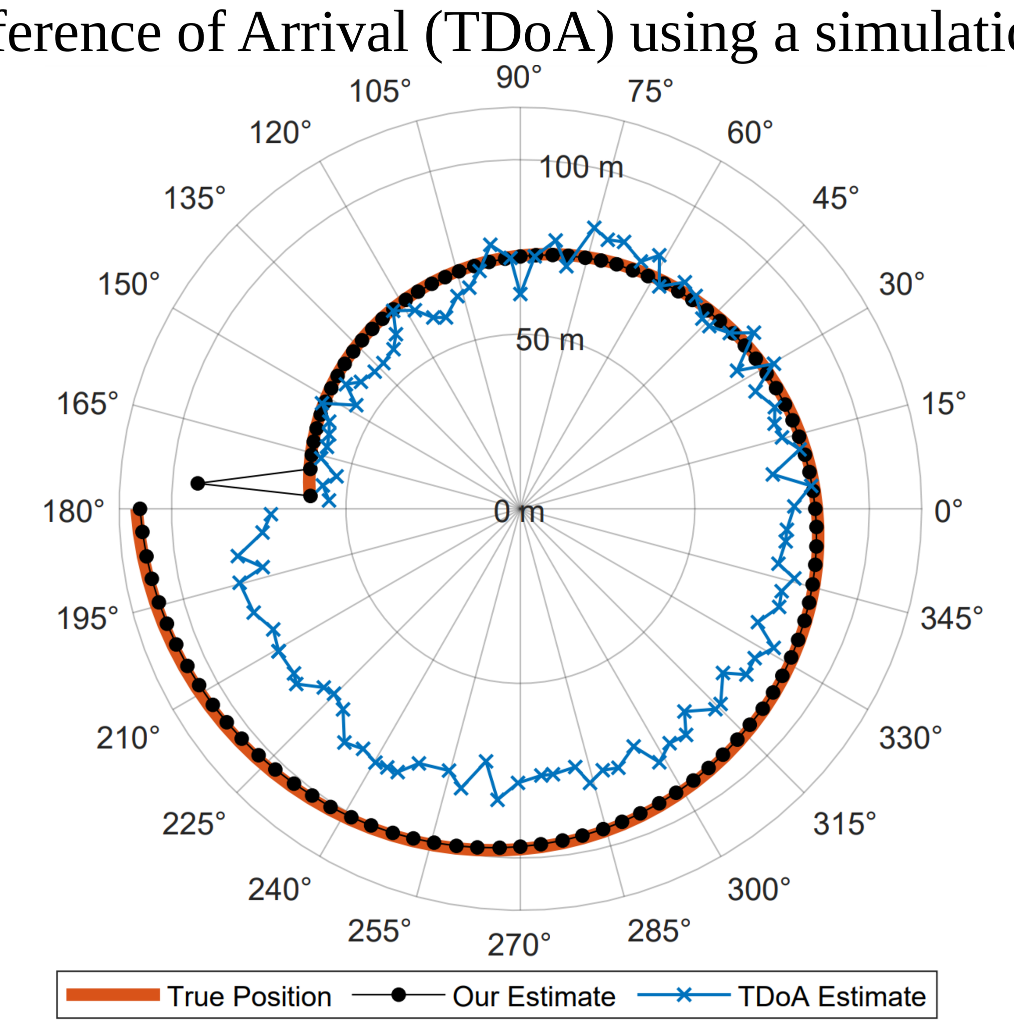

Fig. 6: TDoA vs. Proposed Algorithm Estimation Results

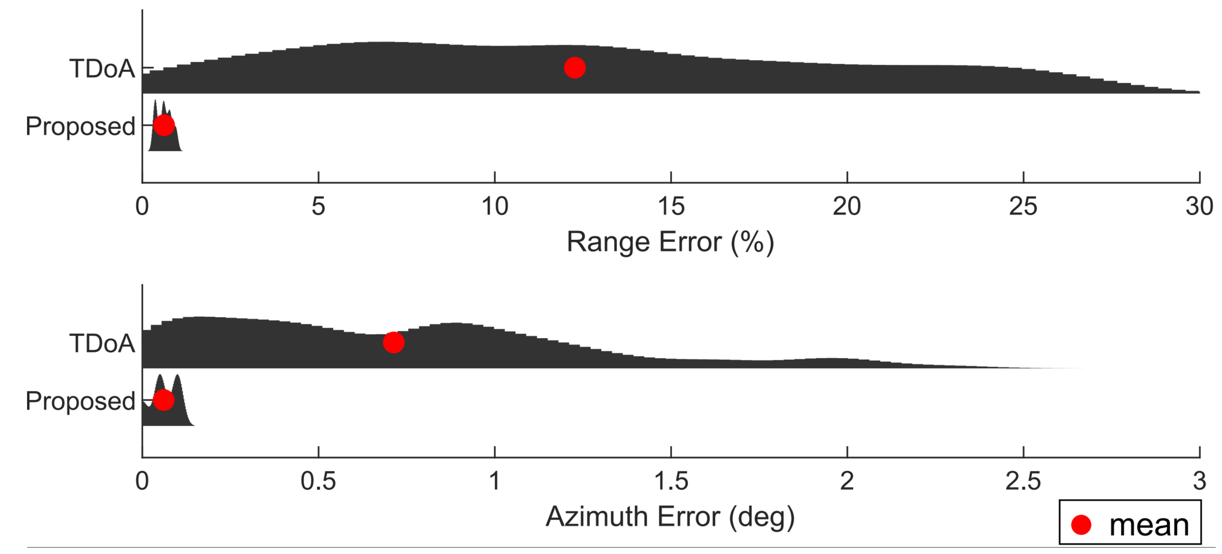

Fig. 7: TDoA vs. Proposed Algorithm Error Distribution

Conclusion

- Accuracy of the implemented SoC was evaluated by comparing the ambiguity function obtained using the FPGA and a MATLAB simulation.
- System runs in real-time using four sensors, with an additional sensor for added redundancy.

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